AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. - 24. (cancelled).

25. (new) A system semiconductor device, comprising:

a system LSI cell portion which includes a plurality of functional blocks for realizing specific functions, each of the functional blocks serving as a unit circuit and being arranged on a semiconductor chip; and

a global wiring layer which at least has conductor means formed in a substrate and a wiring layer of a single-layer or a multi-layer structure formed on the conductor means and which is laminated with the system LSI cell portion so that the functional blocks are electrically connected to each other.

26. (new) A system semiconductor device as claimed in claim 25, wherein the global wiring layer has a varied via as the conductor means formed in the semiconductor substrate, a first wiring layer formed on the buried via, an insulating layer formed on the first wiring layer, a second wiring layer formed on the insulating layer and electrically connected to the first wiring layer through the via, and an adhesive layer formed on the

insulating layer in an area where the second wiring layer is not formed.

27. (new) A system semiconductor device as claimed in claim 25, wherein the global wiring layer has a buried via as the conductor means formed in the semiconductor substrate, a first wiring layer formed on the buried via, an insulating layer formed on the first wiring layer, a second wiring layer formed on the insulating layer and electrically connected to the first wiring layer through the via, and an inner bump formed on a surface of the second wiring layer.

28. (new) A system semiconductor device as claimed in claim 25, wherein the global wiring layer has a secondary wiring layer as the conductor means formed in the substrate made of an organic material, a first wiring layer formed on the secondary wiring layer, an insulating layer formed on the first wiring layer, a second wiring layer formed on the insulating layer and electrically connected to the first wiring layer through a via, and an adhesive layer formed on the insulating layer in an area where the second wiring layer is not formed.

29. (new) A system semiconductor device as claimed in claim 25, wherein the global wiring layer has a secondary wiring layer as the conductor means formed in the substrate made of an organic material, a first wiring layer formed on the secondary wiring layer, an insulating layer formed on the first wiring

layer, a second wiring layer formed on the insulating layer and electrically connected to the first wiring layer through the via, and an inner bump formed on a surface of the second wiring layer.

30. (new) A system semiconductor device as claimed in claim 27, wherein a gap is present between the global wiring layer and a circuit surface of the LSI cell portion connected by the inner bump.

31. (new) A system semiconductor device as claimed in claim 25, wherein the global wiring layer has a bump which is arranged on a substrate surface on the side where the wiring layer is not formed and which is adapted to be electrically connected to an external circuit through the conductor means.

32. (new) A system semiconductor device as claimed in claim 25, wherein the global wiring layer has one or more wiring layers as the wiring layer.

33. (new) A system semiconductor device as claimed in claim 25, wherein the global wiring layer has one or more insulating layers as the insulating layer.

34. (new) A system semiconductor device as claimed in claim 25, wherein:

a plurality of the system LSI cell portions are formed on a semiconductor wafer;

a plurality of the global wiring layers are formed on the semiconductor substrate; and

the semiconductor wafer and the semiconductor substrate are laminated, diced and separated to obtain a plurality of the system semiconductor devices.

35. (new) A method of manufacturing a system semiconductor device, comprising the steps of:

fabricating a system LSI cell portion by forming, on a semiconductor chip, a plurality of functional blocks which serve as unit circuits for realizing specific functions;

fabricating a global wiring layer by forming conductor means in a substrate and forming a wiring layer of a single-layer or a multi-layer structure on the conductor means, and

laminating the system LSI cell portion with the global wiring layer.

36. (new) A method as claimed in claim 35, wherein the global wiring layer is obtained by the steps of forming a buried via as the conductor means in the semiconductor substrate, forming a first wiring layer on the buried via, forming an insulating layer on the first wiring layer, forming, on the insulating layer, a second wiring layer electrically connected to the first wiring layer through the via, and forming an adhesive layer on the insulating layer in an area where the second wiring layer is not formed.

37. (new) A method as claimed in claim 35, wherein the global wiring layer is obtained by the steps of forming a buried

via as the conductor means in the semiconductor substrate, forming a first wiring layer on the buried via, forming an insulating layer on the first wiring layer, forming, on the insulating layer, a second wiring layer electrically connected to the first wiring layer through the via, and forming an inner bump on a surface of the second wiring layer.

38. (new) A method as claimed in claim 35, wherein the global wiring layer is obtained by the steps of forming a secondary wiring layer as the conductor means in the substrate made of an organic material, forming a first wiring layer on the secondary wiring layer, forming an insulating layer on the first wiring layer, forming, on the insulating layer, a second wiring layer electrically connected to the first wiring layer through a via, and forming an adhesive layer on the insulating layer in an area where the second wiring layer is not formed.

39. (new) A method as claimed in claim 35, wherein the global wiring layer is obtained by the steps of forming a secondary wiring layer as the conductor means in the substrate made of an organic material, forming a first wiring layer on the secondary wiring layer, forming an insulating layer on the first wiring layer, forming, on the insulating layer, a second wiring layer electrically connected to the first wiring layer through a via, and forming an inner bump on a surface of the second wiring layer.

40. (new) A method as claimed in claim 37, wherein the global wiring layer and a circuit surface of the LSI cell portion are connected by the inner bump with a gap left therebetween.

41. (new) A method as claimed in claim 35, wherein the global wiring layer is obtained by further forming a bump which is arranged on a substrate surface on the side where the wiring layer is not formed and which is adapted to be electrically connected to an external circuit through the conductor means.

42. (new) A method as claimed in claim 35, wherein the global wiring layer has one or more wiring layers as the wiring layer.

43. (new) A method as claimed in claim 35, wherein the global wiring layer has one or more insulating layers as the insulating layer.

44. (new) A method as claimed in claim 35, comprising the steps of forming a plurality of the system LSI cell portions on a semiconductor wafer, forming a plurality of the global wiring layers on the semiconductor substrate, laminating the semiconductor wafer and the semiconductor substrate, and dicing and separating the laminated semiconductor wafer and the semiconductor substrate to obtain a plurality of the system semiconductor devices.

45. (new) A system semiconductor device as claimed in claim 29, wherein a gap is present between the global wiring

layer and a circuit surface of the LSI cell portion connected by the inner bump.

46. (new) A method as claimed in claim 39, wherein the global wiring layer and a circuit surface of the LSI cell portion are connected by the inner bump with a gap left therebetween.

47. (new) A system semiconductor device, comprising:

a system LSI cell portion which includes a plurality of functional blocks for realizing specific functions and which has pads formed on the functional blocks, each of the functional blocks serving as a unit circuit and being arranged on a semiconductor chip; and

a global wiring layer which has a wiring layer on a semiconductor substrate and which is laminated with the system LSI cell portion such that the functional blocks are electrically connected to each other;

the global wiring layer comprises;

a first wiring layer formed on the semiconductor substrate,

an insulating layer formed on the first wiring layer,

a second wiring layer formed on the insulating layer,

a first via which is formed in the insulating layer and which electrically connects the first wiring layer with the second wiring layer, and

a second via which is buried in the semiconductor substrate and which is electrically connected to the first wiring layer and which serves as en electrode for an external circuit,

the global wiring layer being laminated with the system LSI portion by electrically connecting the functional blocks with the second wiring layer through the pads so that the functional blocks are electrically connected to the external circuit through the first wiring layer and the second wiring layer.